

1. Description

BL19N40, the silicon N-channel Enhanced MOSFETs, is obtained by advanced MOSFET technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor is suitable device for SMPS, high speed switching and general purpose applications.

KEY CHARACTERISTICS

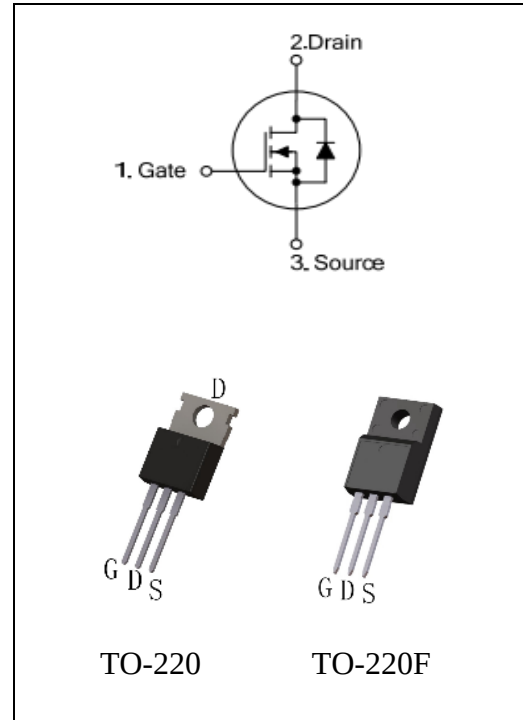
Parameter	Value	Unit
V_{DS}	400	V
I_D	19	A
$R_{DS(ON)}$.Typ	0.22	Ω

FEATURES

- Fast Switching
- Low C_{rss}
- 100% avalanche tested
- Improved dv/dt capability
- RoHS product

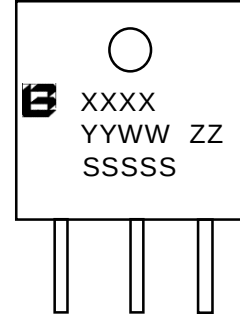
APPLICATIONS

- High frequency switching mode power supply
- Electronic ballast



ORDERING INFORMATION

Ordering Codes	Package	Product Code	Packing
BL19N40-P	TO-220	19N40	Tube
BL19N40-A	TO-220F		Tube

BL19N40-A (2) Package type (1) Chip name (1) BL19N40: 400V 19A (2) A:TO-220F P:TO-220	 XXXX: Product Code YYWW: Year&Week ZZ: Assembly Code SSSSS: Lot Code
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2. ABSOLUTE RATINGS

 at $T_C = 25^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Units
V_{DS}	Drain-to-Source Voltage	400	V
I_D	Continuous Drain Current	19	A
	Continuous Drain Current $T_C = 100^{\circ}\text{C}$	12.6	A
I_{DM}	Pulsed Drain Current(Note1)	76	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy(Note2)	900	mJ
dv/dt	Peak Diode Recovery dv/dt (Note3)	5.0	V/ns
P_D	Power Dissipation TO-220	278	W
	Derating Factor above 25°C	2.2	W/ $^{\circ}\text{C}$
P_D	Power Dissipation TO-220F	62	W
	Derating Factor above 25°C	0.5	W/ $^{\circ}\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	$^{\circ}\text{C}$
T_L	Maximum Temperature for Soldering	300	$^{\circ}\text{C}$

3. Thermal characteristics

Thermal characteristics TO-220

Symbol	Parameter	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	0.45	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	62.5	$^{\circ}\text{C}/\text{W}$

Thermal characteristics TO-220F

Symbol	Parameter	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	2	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	62.5	$^{\circ}\text{C}/\text{W}$

4. Electrical Characteristics

 at $T_C = 25^\circ\text{C}$, unless otherwise specified

OFF Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	400	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250\mu A$, Reference 25°C	--	0.45	--	V/ $^\circ\text{C}$
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=400V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	--	--	1	μA
		$V_{DS}=320V$, $V_{GS}=0V$, $T_J=125^\circ\text{C}$	--	--	10	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V$, $I_D=4A$ (Note4)	--	0.22	0.27	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu A$ (Note4)	2	3	4	V
g_{fs}	Forward Transconductance	$V_{DS}=15V$, $I_D=9.5A$ (Note4)	--	10.0	--	S

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
R_g	Gate resistance	$f=1.0\text{MHz}$	--	1.4	--	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V$ $V_{DS}=25V$ $f=1.0\text{MHz}$	--	2300	--	PF
C_{oss}	Output Capacitance		--	210	--	
C_{rss}	Reverse Transfer Capacitance		--	3.3	--	

Switching Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	ID =19A VDD = 250V VGS = 10V RG =10Ω	--	32	--	ns
t_r	Rise Time		--	26	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	80	--	
t_f	Fall Time		--	35	--	
Q_g	Total Gate Charge	ID =19A VDD =320V VGS = 10V	--	40	--	nC
Q_{gs}	Gate to Source Charge		--	12.5	--	
Q_{gd}	Gate to Drain ("Miller")Charge		--	10.5	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Values			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	TC=25 °C	--	--	19	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	76	A
V_{SD}	Diode Forward Voltage	IS=19A, VGS=0V(Note4)	--	--	1.2	V
T_{rr}	Reverse Recovery Time	IS=19A, Tj = 25°C dIF/dt=100A/us, VGS=0V	--	285	--	ns
Q_{rr}	Reverse Recovery Charge		--	3900	--	nC

Note1: Pulse width limited by maximum junction temperature

Note2: L=10mH, VD=50V, Start TJ=25°C

Note3: ISD =19A, di/dt ≤100A/us, VDD≤BVDS, Start TJ=25°C

Note4: Pulse width tp≤300μs, δ≤2%

5. Characteristics Curves

Figure 1a Safe Operating Area (No FullPAK)

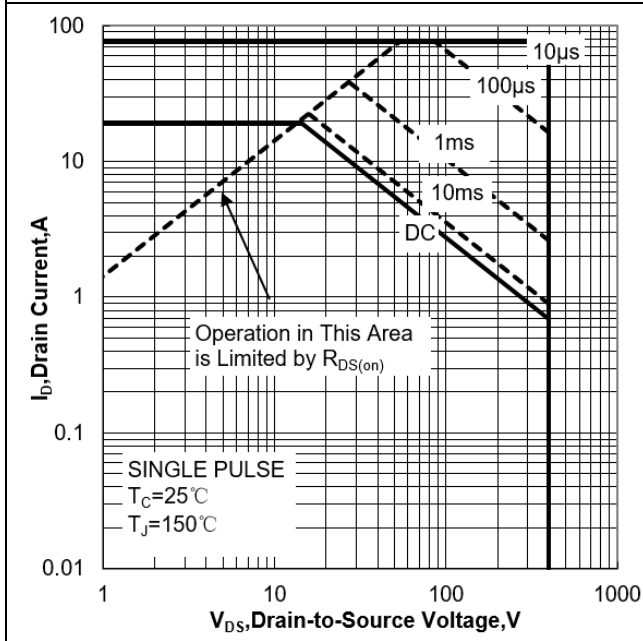


Figure 1b Safe Operating Area (FullPAK)

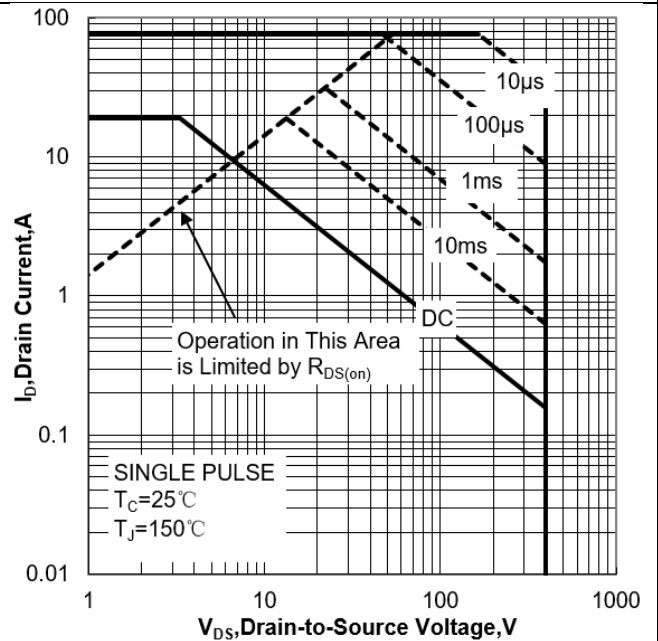


Figure 2a Power Dissipation (No FullPAK)

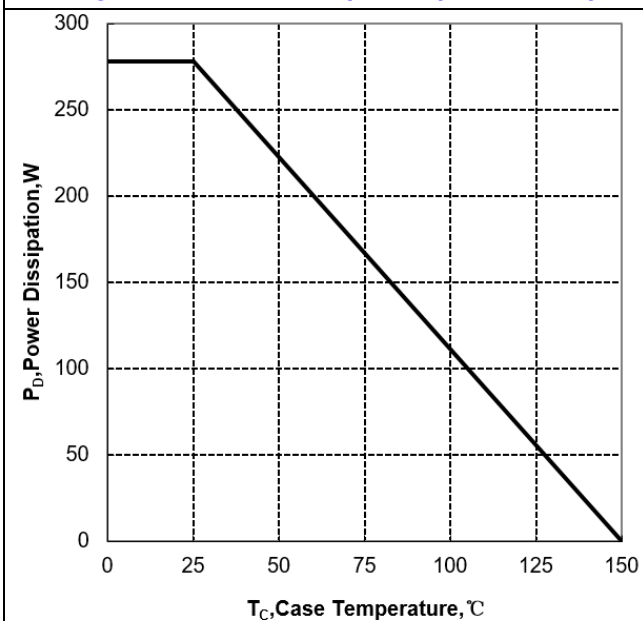


Figure 2b Power Dissipation (FullPAK)

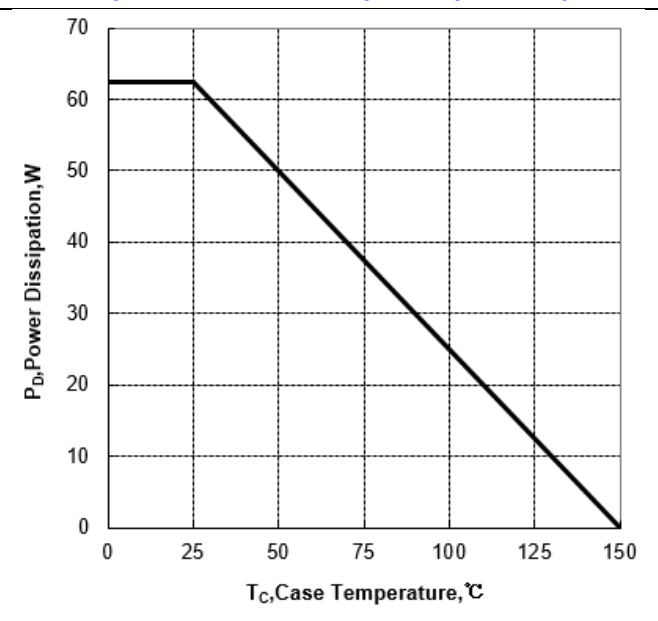


Figure 3a Max Thermal Impedance (No FullPAK)

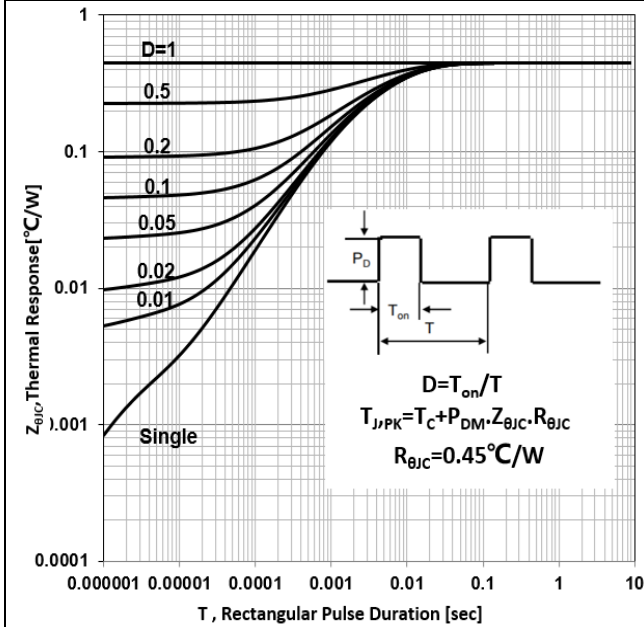


Figure 3b Max Thermal Impedance (FullPAK)

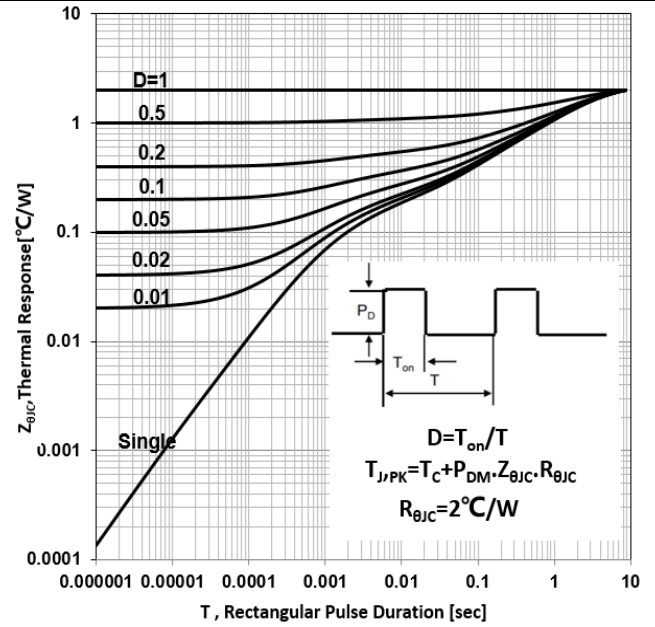


Figure 4 Typical Output Characteristics

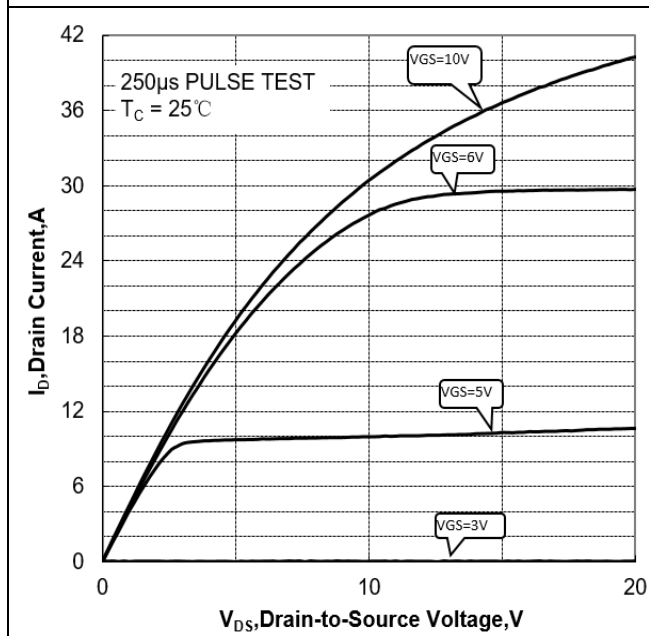


Figure 5 Typical Transfer Characteristics

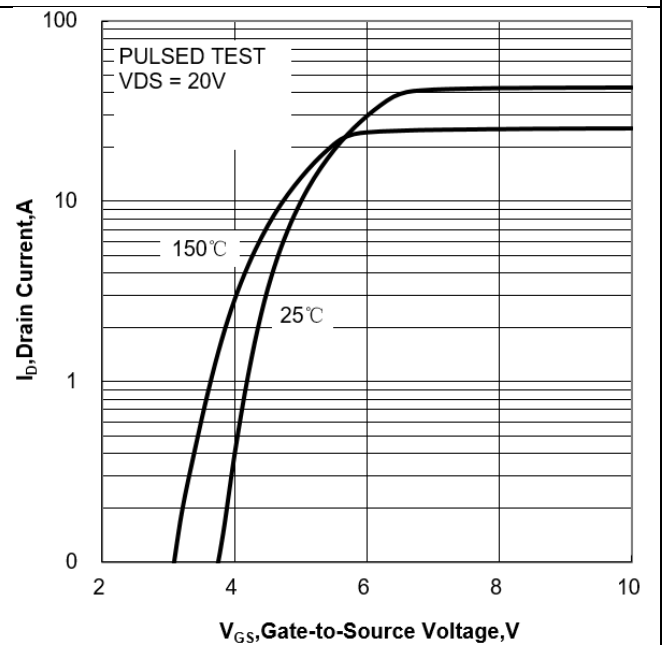


Figure 6 Typical Drain to Source ON Resistance vs Drain Current

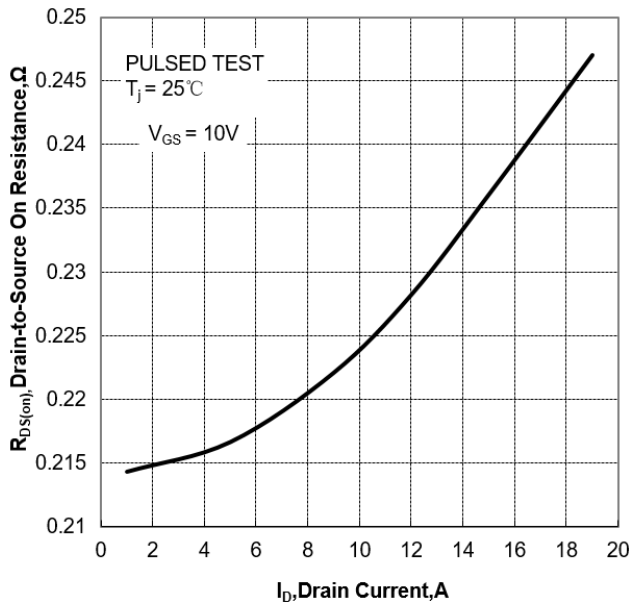


Figure 7 Typical Drian to Source on Resistance vs Junction Temperature

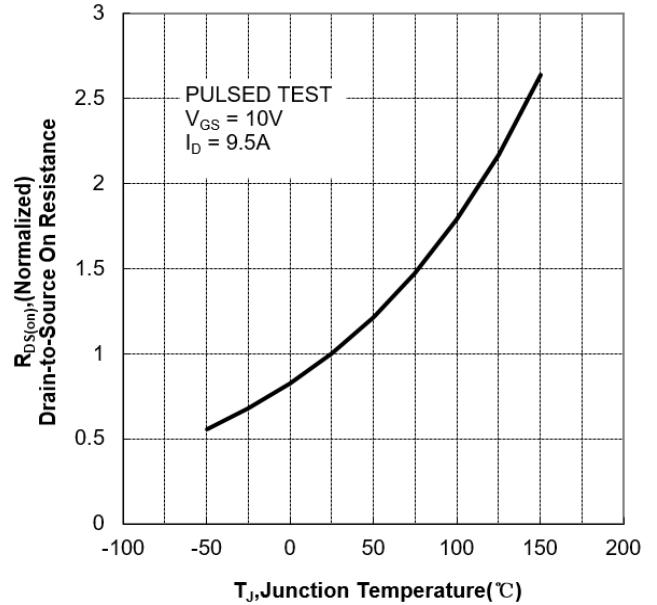


Figure 8 Typical Theshold Voltage vs Junction Temperature

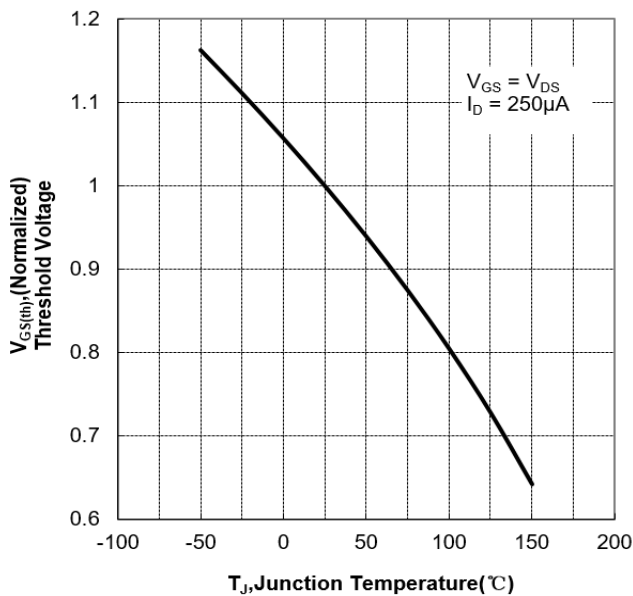


Figure 9 Typical Breakdown Voltage vs Junction Temperature

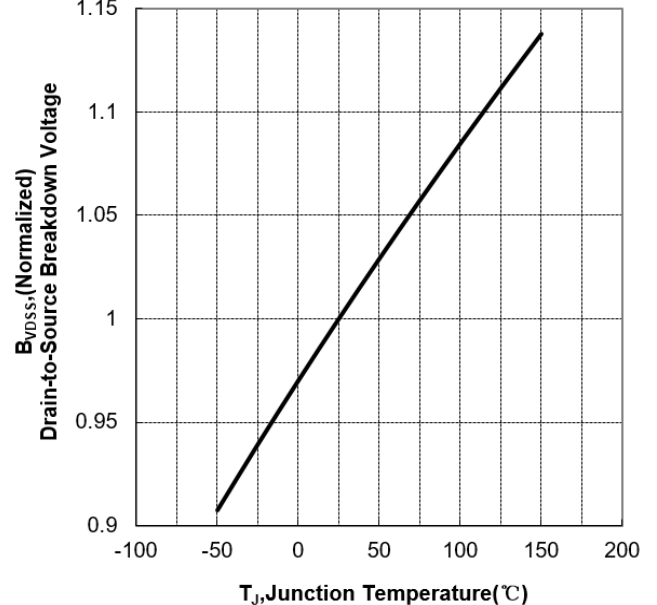


Figure 10 Typical Capacitance vs Drain to Source Voltage

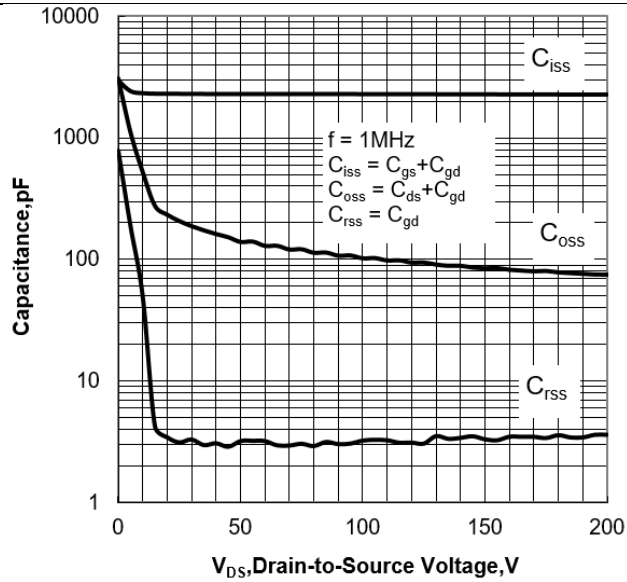
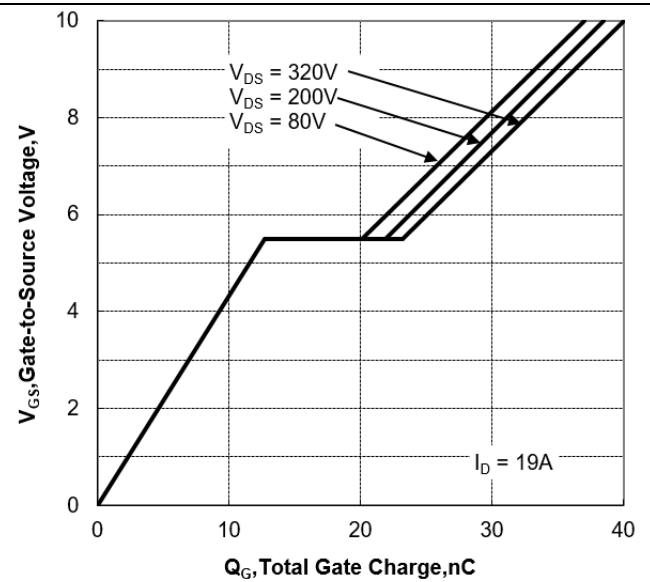
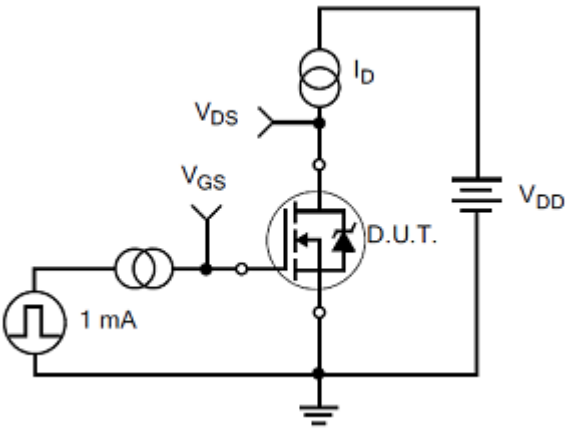
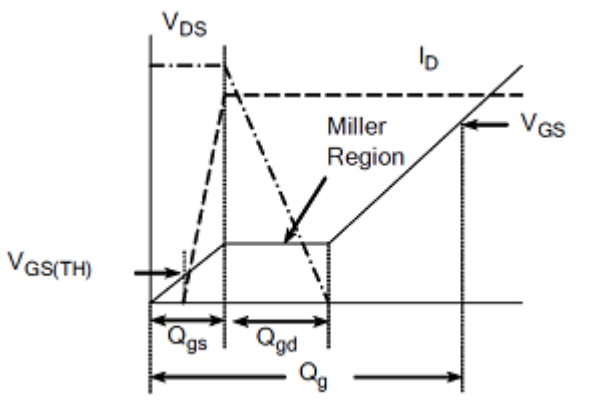
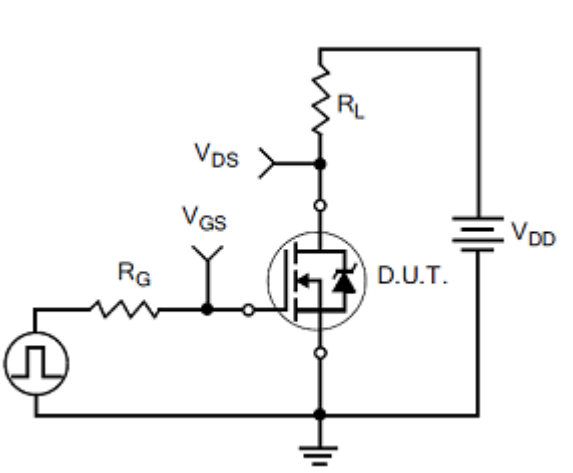
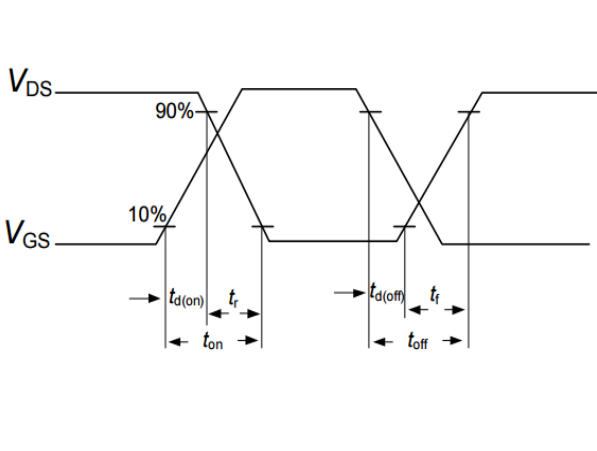


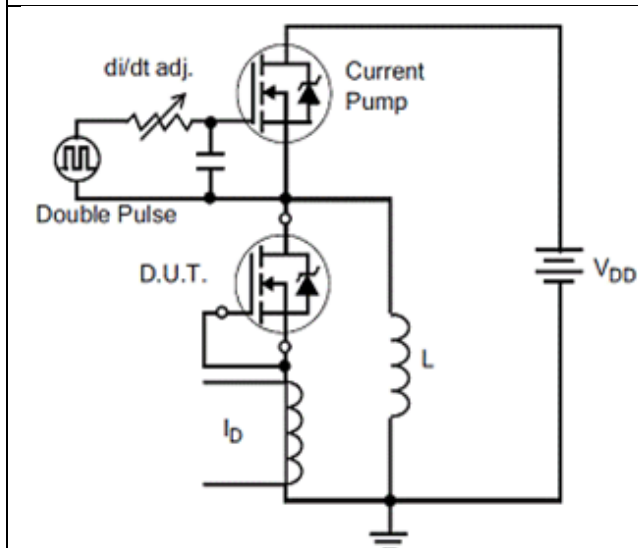
Figure 11 Typical Gate Charge vs Gate to Source Voltage



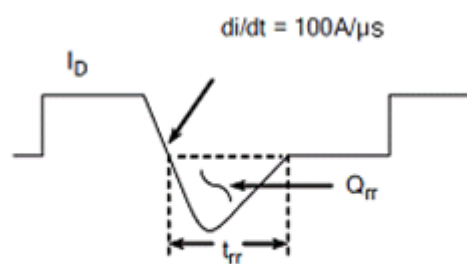
6. Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Waveforms
 The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The gate is driven by a 1 mA current source. The drain is connected to a load resistor and a drain current source I_D. The gate is connected to a gate voltage source V_{GS}. The drain is connected to a drain voltage source V_{DS}. The MOSFET is connected to a supply voltage V_{DD}.	 The diagram shows the relationship between V_{DS}, I_D, and V_{GS} during a gate charge test. The V_{GS} waveform is shown with three regions: the linear region, the Miller Region (where V_{DS} is constant and V_{GS} increases), and the saturation region. The gate charge Q_g is the total area under the V_{GS} curve. The gate charge Q_{gs} is the area under the V_{GS} curve in the linear region. The gate charge Q_{gd} is the area under the V_{GS} curve in the Miller Region. The threshold voltage $V_{GS(TH)}$ is indicated.
Resistive Switching Test Circuit	Resistive Switching Waveforms
 The diagram shows a MOSFET (D.U.T.) in a common-source configuration. The gate is driven by a current source I_G through a gate resistor R_G. The drain is connected to a load resistor R_L. The gate is connected to a gate voltage source V_{GS}. The drain is connected to a drain voltage source V_{DS}. The MOSFET is connected to a supply voltage V_{DD}.	 The diagram shows the switching waveforms for V_{DS} and V_{GS}. The V_{GS} waveform is shown with a rising edge (turn-on) and a falling edge (turn-off). The V_{DS} waveform is shown with a falling edge (turn-on) and a rising edge (turn-off). The turn-on time t_{on} is the time from 10% to 90% of V_{GS} rising. The turn-off time t_{off} is the time from 90% to 10% of V_{GS} falling. The delay time $t_{d(on)}$ is the time from 10% of V_{GS} rising to 90% of V_{DS} falling. The delay time $t_{d(off)}$ is the time from 90% of V_{GS} falling to 90% of V_{DS} rising. The rise time t_r is the time from 90% to 100% of V_{GS} rising. The fall time t_f is the time from 100% to 90% of V_{GS} falling.

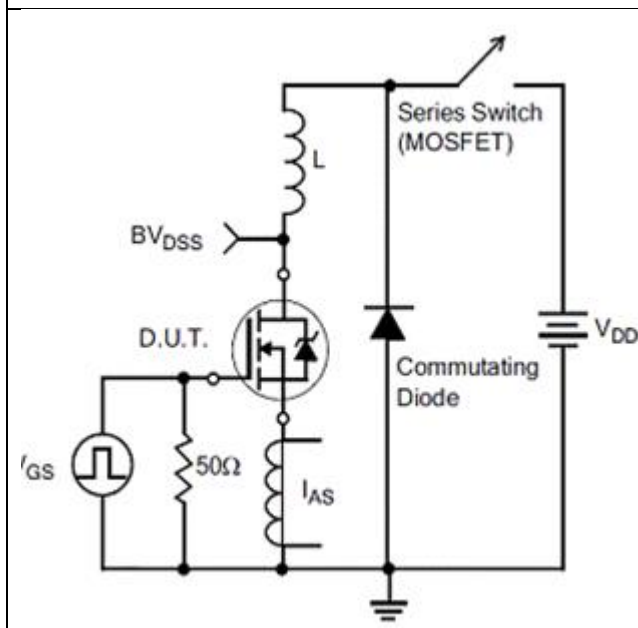
Diode Reverse Recovery Test Circuit



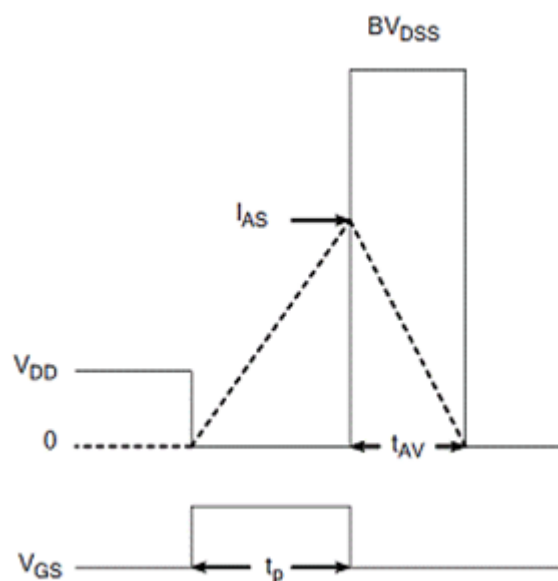
Diode Reverse Recovery Waveform



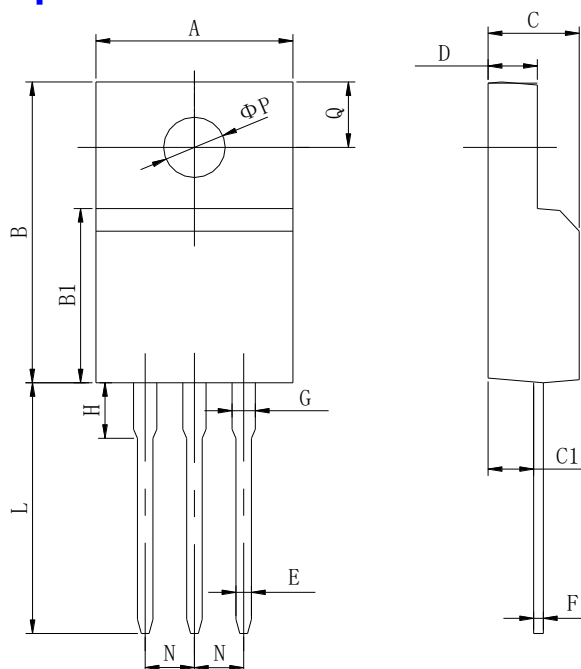
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveform

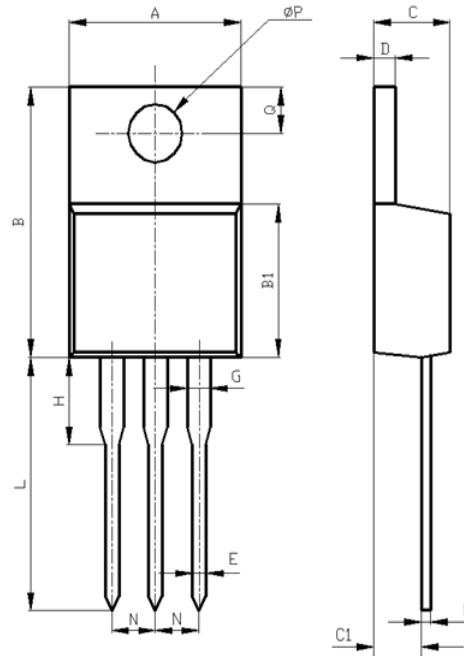


7. Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	1.60	2.90
L	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
Φ P	2.90	3.30

TO-220F Package



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
Φ P	3.50	3.90

TO-220 Package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shanghai Belling reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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